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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/687,907	10/17/2003	David P. Hannum	10971353-3	1941

22879 7590 04/20/2006

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EXAMINER	
TRAN, DENISE	

ART UNIT	PAPER NUMBER
2185	

DATE MAILED: 04/20/2006

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BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Application Number: 10/687,907
Filing Date: October 17, 2003
Appellant(s): HANNUM ET AL.

Fogarty, III J. Michael
For Appellant

EXAMINER'S ANSWER

This is in response to the appeal brief filed 11/10/05 appealing from the Office action mailed 06/17/05.

(1) Real Party in Interest

A statement identifying by name the real party in interest is contained in the brief.

(2) Related Appeals and Interferences

The examiner is not aware of any related appeals, interferences, or judicial proceedings which will directly affect or be directly affected by or have a bearing on the Board's decision in the pending appeal.

(3) Status of Claims

The statement of the status of claims contained in the brief is correct.

(4) Status of Amendments After Final

No amendment after final has been filed.

(5) Summary of Claimed Subject Matter

The summary of claimed subject matter contained in the brief is correct.

(6) Grounds of Rejection to be Reviewed on Appeal

GROUNDS OF REJECTION NOT ON REVIEW

The following grounds of rejection have not been withdrawn by the examiner, but they are not under review on appeal because they have not been presented for review in the appellant's brief.

Claims 1-3, 6-13, and 16-18 are rejected under a judicial created doctrine of obviousness-type double patenting as being unpatentable over claims 1-16 of U.S. Patent No. 6,823,434.

(7) Claims Appendix

The copy of the appealed claims contained in the Appendix to the brief is correct.

(8) Evidence Relied Upon

5,809,528	Miller et al.	9-1998
6,539,541	Geva et al.	03-2003
6,564,317	Hale et al.	05-2003
6,823,434	Hannum et al.	11-2004

(9) Grounds of Rejection

The following ground(s) of rejection are applicable to the appealed claims:

1. The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. See *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970);and, *In re Thorington,* 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent is shown to be commonly owned with this application. See 37 CFR 1.130(b).

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

2. Claim(s) 1-16 of patent No. US 6,823,434 contain(s) every element of claim(s) 1-3, 6-13, and 16-18 of the instant application and as such anticipate(s) claim(s) 1-3, 6-13, and 16-18 of the instant application.

instant application	US 6,823,434
1. A method for preventing matching of prospective entries with table entries stored in a fully associative table, the method comprising the step of: Writing illegal values to substantially all of said table entries in said fully associative table; and Prohibiting said prospective entries from having said illegal values under normal program execution conditions,. thereby preventing any matching conditions between said table entries and said prospective entries.	1. A method for preventing matching of prospective entries with table entries stored in a fully associative table the method comprising: Writing illegal values to substantially all of said table entries in said fully associative table; Prohibiting said prospective entries from having said illegal values under normal program execution conditions, thereby preventing any matching conditions between said table entries and said prospective entries; Wherein said writing step comprises the steps of: Setting at least one type bit to 1;

	and all of a set of frames bits to 1.

11. A system for preventing matching of prospective entries with table entries stored in a fully associative table, the system comprising:	10. A system for preventing matching of prospective entries with table entries stored in a fully associative table, the system comprising:
means for writing illegal values to substantially all of said table entries in said fully associative table, and	means for writing illegal values to substantially all of said table entries in said fully associative table, comprising means for setting at least one type bit to 1, and means for setting all of a set of frame bits to 1; and
means for prohibiting said prospective entries from having said illegal values, thereby preventing any matching conditions between said table entries and said prospective entries.	means for prohibiting said prospective entries from having said illegal values, thereby preventing any matching conditions between said table entries and said prospective entries.
As per claims 2 and 12, said writing step is performed during power up of a system.	As per claims 2 and 11, said writing step is performed during power up of a system
As per claims 3 and 13, said writing step initiated by executing a specific machine specific instruction.	As per claims 3 and 12, said writing step initiated by executing a specific machine specific instruction.

As per claims 6 and 16, said fully associative table is included in a system for finding and validating data most recent advanced load instruction for a given check instruction.	As per claims 5 and 14, said fully associative table is included in a system for finding and validating data most recent advanced load instruction for a given check instruction.
As per claims 7 and 17, updating entries in a fully associative table employing a pointer to indicate a first table location containing an invalid entry.	As per claims 6 and 15, updating entries in a fully associative table employing a pointer to indicate a first table location containing an invalid entry.
As per claims 8 and 18, storing memory addresses in said fully associative table.	As per claims 7 and 16, storing memory addresses in said fully associative table.
As per claim 9, storing register numbers in said fully associative.	As per claim 8, storing register numbers in said fully associative.
As per claim 10, issuing a force update command, thereby causing a plurality of entry locations in said fully associative table to acquire predetermined illegal value.	As per claim 9, issuing a force update command, thereby causing a plurality of entry locations in said fully associative table to acquire predetermined illegal value.

"A later patent claim is not patentably distinct from an earlier patent claim if the later claim is obvious over, or **anticipated by**, the earlier claim. In re Longi, 759 F.2d at 896, 225 USPQ at 651 (affirming a holding of obviousness-type double patenting because the claims at issue were obvious over claims in four prior art patents); In re Berg, 140 F.3d at 1437, 46 USPQ2d at 1233 (Fed. Cir. 1998) (affirming a holding of obviousness-type double patenting where a patent application claim to a genus is anticipated by a patent claim to a species within that genus). " ELI LILLY AND COMPANY v BARR LABORATORIES, INC., United States Court of Appeals for the Federal Circuit, ON PETITION FOR REHEARING EN BANC (DECIDED: May 30, 2001).

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claims 1-2, 7-8, 10-12, and 17-19 are rejected under 35 U.S.C. 102(b) as being anticipated by Miller et al., U.S. Patent No. 5,809,528 (hereinafter Miller).

As per claim 19, Miller teaches a system for disabling matching of prospective entries with tables entries resident in a fully associative table (e.g., col. 15, lines 35-60; col. 11, lines 55-65), the system comprising: a plurality of entry locations in said fully associative table (e.g., fig. 1, el. 104; col. 11, line 55-65); and a force update command for causing said plurality of entry locations to acquire predetermined illegal bit values not present in prospective entries at ports connected to said fully associative table (e.g., col. 15, lines 35-50; col. 16, lines 10-15).

As per claims 1 and 11, Miller teaches a method/system for preventing matching of prospective entries with table entries stored in a fully associative table (e.g., col. 15, lines 40-50), the method/system comprising:

Writing illegal values to substantially all of said table entries in said fully associative table (e.g., col. 15, lines 40-60 and col. 16, lines 10-15);

Prohibiting said prospective entries from having said illegal values under normal program execution conditions (e.g., col. 11, lines 55-60 and col. 15, lines 45-46), thereby preventing any matching conditions between said table entries and said prospective entries (e.g. col. 15, lines 40-50).

As per claims 8 and 18, Miller shows storing memory addresses in said fully associative table (e.g. col. 15, lines 40-50).

As per claims 2 and 12, Miller teaches writing to be performed during power up of a system (e.g., col. 15, lines 35-50).

As per claims 7 and 17, Miller teaches updating entries in a fully associative table employing a pointer to indicate a first table location containing an invalid entry (e.g., col. 16, lines 19-30; i.e., an invalid address is a first table location).

As per claim 10, Miller shows a force update command for causing a plurality of entry locations in a table to acquire predetermined illegal value (e.g., col. 15, lines 35-45; col. 5, lines 15-40).

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 6, 9, and 16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Miller et al., U.S. Patent No. 5,809,528 (hereinafter Miller), in view of Geva, U.S. 6539541, (hereinafter Geva).

As per claims 6, 9, and 16, Miller shows the fully associative table (e.g., fig. 1; col. 11, lines 55-60) for finding and validating data (e.g., fig. 1; col. 11, lines 55-60). Miller does not explicitly shows a most recent advanced load instruction for a given check instruction or storing register numbers. Geva shows a most recent advanced load instruction for a given check instruction (e.g., col. 14, lines 15-65) and storing register numbers (e.g., col. 14, lines 20-30). It would have been obvious to one of ordinary skill in the art at the time the invention was made to apply the teaching of Geva into the system of Miller because it would allow handling advanced loads in a cache system; thereby, increasing the performance and speed processing of the system.

7. Claims 3 and 13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Miller et al., U.S. Patent No. 5,809,528 (hereinafter Miller), in view of Hale et al., U.S. 6564317, (hereinafter Hale).

As per claims 3 and 13, Miller does not explicitly show said writing step is initiated by executing a specific machine specific instruction. Hale shows writing step initiated by executing a specific machine specific instruction (e.g., col. 9, lines 30-45). It

would have been obvious to one of ordinary skill in the art at the time the invention was made to apply the teaching of Hale into the system of Miller because it would allow a secure boot process when performing initialization of a computer system upon power up or system reset.

(10) Response to Argument

1. In the Argument, the Appellant argued (1) that a Terminal Disclaimer will be in compliance with 37 C.F.R. 1.321(b), if the Non –statutory Double Patenting rejection with respect to claims 1-3, 6-13, and 16-19 as being unpatentable over claims 1-16 of U.S. patent No. 6,823,434 still properly stands, upon an indication of allowability on all other matters.

In response to the Appellant's argument (1), the Non-statutory Double Patenting rejection is deemed to be proper. Therefore, it is maintained until a timely filed Terminal Disclaimer in compliance with 37 CFR 1.321(c) to be submitted.

2. In the Argument, Appellant argued (2) that Miller 's invalid state is not the same limitation as the claimed illegal value and Miller, col. 15, lines 42-45, teaches "at initialization . . . all valid status bits are initialized to an invalid state," but does not teach "writing illegal values to substantially all of said table entries in said fully associative table," claim 1 and "means for writing illegal values to substantially all of said table entries in said fully associative table, " claim 11.

The examiner disagreed with the Appellant's arguments (2). First, Miller's invalid state is the same limitation as the claimed illegal value because Miller's invalid state indicates content of a cache table entry is not allowed to use and causes a miss (i.e., no match) in the cache (i.e., illegal; e.g., col. 3, lines 25-30; col. 15, lines 44-46).

Next, Miller's invalid state is the claimed illegal value as defined in the present specification, page 8, lines 21-22, "a value which a prospective entry would not acquire in a normal course of program execution," since Miller, col. 15, lines 40-50 discloses a value (i.e., invalid state) is acquired in "an initialization" which is not a normal course of program execution. In another words, Miller teaches the value is not acquired in a normal course of program execution as the claimed illegal value.

In addition, Miller teaches a value (i.e., invalid state) which a prospective entry (i.e., a requested entry at port) would not acquire in a normal course of program execution as defined in the present specification, page 8, lines 21-22 because Miller, col. 10, lines 25-30; col. 15, lines 45-50, teaches the prospective entry (i.e., a requested system address, data needed) only has address bits, data bits at ports and does not have an invalid value at the ports in a normal course program execution. Therefore, because Miller's prospective entry would not acquired the invalid value in a normal course program, Miller' invalid value is the claimed illegal value.

In short, because Miller's invalid state is the claimed illegal value; the teaching "at initialization . . . all valid status bits are initialized to an invalid state," Miller, col. 15, lines 42-45 and " fully associate cache tag structure," Miller, col. 11, lines 55-60 are read on "writing illegal values to substantially all of said table entries in said fully associative

table," claim 1 and "means for writing illegal values to substantially all of said table entries in said fully associative table, " claim 11.

3. In the Argument, the Appellant's argued (3) that Miller's invalid value which is a non-current, old, or stale value is acquired during the normal course of program execution, whereas the claimed illegal value is defined in the present specification, page 8, lines 21-22 as "a value which prospective entry would preferably not acquire in normal course of program execution."

The examiner disagreed with the Appellant's argument (3). First of all, the specification page 8, lines 21-22, stated "**preferably**" but not only; therefore, the claimed illegal value don't have to limit itself to "not acquire in a normal course program" only at all the times. Next, according to col. 15, lines 40-50, Miller discloses a value (i.e., invalid value) is acquired in "an initialization" which is not a normal course of program execution. In another words, Miller teaches the value is not acquired in a normal course of program execution as the claimed illegal value. Therefore, Miller's invalid value is the claimed illegal value as defined in the cited text of the present specification. Thus, Miller teaches every elements of claims 1 and 11.

In addition, Miller teaches a value (i.e., invalid value) which a prospective entry (i.e., a requested entry at port) would not acquire in a normal course of program execution as defined in the present specification, page, lines 21-22 because Miller, col. 10, lines 25-30; col. 15, lines 40-50, teaches the prospective entry (i.e., a requested system address, data needed) only has address bits, data bits at ports and does not

have an invalid value at the ports in a normal course program execution. Therefore, because Miller's prospective entry would not acquired the invalid value in a normal course program, Miller' invalid value is the claimed illegal value as defined in the cited text of the present specification.

In further discussion, the examiner disagreed with the appellant's argument that Miller's invalid value is a non –current, old or stale value which is acquired during the normal course of program execution. In particular, Miller teaches illegal values (i.e., invalid value) which is acquired when "data no longer be current" and "should not be used" (col. 3, lines 15-25) and when "an address invalidation operation occurs" (col. 16, lines 13-15). Detecting an invalid data and having an address invalidation operation are not a normal course of program execution because "non-current", "stale," and "old" data is not a normal situation in a computer system and needs to be detected to use a special operation which is an invalidation operation (Miller, col. 3, lines 15-25 and col. 16, lines 10-15). Therefore, Miller teaches illegal values which not acquired during a normal course of program execution.

4. In the Argument, the Appellant's argued (4) that Miller does not teach the claimed force update command and the appellant asserted that a force update command for causing a plurality of entry locations to acquire predetermined illegal bit values is not the same limitation as Miller 's system initialization procedure, nor is it the same as Miller's operation for identifying an invalid table entry and setting an invalid entry flag.

The examiner disagreed with the Appellant's arguments (4). As noted in the last office action, page 5, lines 1-2, Miller teaches a force update command for causing said plurality of entry locations to acquire predetermined illegal bit values not present in prospective entries at ports connected to said fully associative table (e.g., col. 15, lines 35-50; col. 16, lines 10-15). According to col. 15, lines 35-50 and col. 16, lines 10-15, Miller teaches a force update command (i.e., on power up, system reset or a "hit" from a snoop/compare operation) for causing said plurality of entry locations to acquire predetermined illegal bit values (i.e. table entries to have predetermined invalid bit values) not present in prospective entries at ports connected to said fully associated table (i.e., the prospective entry only has address bits, data bits at ports and does not have invalid bits at ports).

Also, Miller col. 15, lines 35-50 and col. 16, lines 10-15, teaches "Power up" or "system reset" or a "hit" from snoop/compare operation is a force update command because it causes the plurality of entry locations to acquire predetermined illegal bit values (i.e. table entries to have predetermined invalid bit values) not present in prospective entries at ports connected to said fully associated table (i.e., the prospective entry only has address bits, data bits at ports and does not have invalid bits at ports).

5. In the Argument, the Appellant argued (5) that there is no suggestion to combine the teaching of Miller and Geva.

In response to Appellant's arguments (5) that there is no suggestion to combine the references, the examiner recognizes that obviousness can only be established by

combining or modifying the teachings of the prior art to produce the claimed invention where there is some teaching, suggestion, or motivation to do so found either in the references themselves or in the knowledge generally available to one of ordinary skill in the art. See *In re Fine*, 837 F.2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988)and *In re Jones*, 958 F.2d 347, 21 USPQ2d 1941 (Fed. Cir. 1992). In this case, Miller shows the fully associative table (e.g., fig. 1; col. 11, lines 55-60) for finding and validating data (e.g., fig. 1; col. 11, lines 55-60). Miller does not explicitly shows a most recent advanced load instruction for a given check instruction or storing register numbers. Geva shows a most recent advanced load instruction for a given check instruction (e.g., col. 14, lines 15-65) and storing register numbers (e.g., col. 14, lines 20-30). It would have been obvious to one of ordinary skill in the art at the time the invention was made to apply the teaching of Geva into the system of Miller because it would allow handling advanced loads in a cache system; thereby, increasing the performance and speed processing of the system.

6. In the Argument, the Appellant argued.(6) that there is no suggestion that Miller 's method for handling invalid data in a memory is combinable with Geva's method of compiling a loop instruction.

The examiner disagreed with the Appellant's argument (6) because both Miller and Geva teach the use of a cache table for handling data. In particular, Miller teaches the use of a fully associate cache table (e.g., col. 11, lines 55-60) and Geva teaches the

use of a cache table for storing register numbers and for validating a most recent advanced load instruction (e.g., col. 14, lines 15-65).

Also, Miller shows the fully associative table (e.g., fig. 1; col. 11, lines 55-60) for finding and validating data (e.g., fig. 1; col. 11, lines 55-60). Miller does not explicitly shows a most recent advanced load instruction for a given check instruction or storing register numbers. Geva shows a most recent advanced load instruction for a given check instruction (e.g., col. 14, lines 15-65) and storing register numbers (e.g., col. 14, lines 20-30). It would have been obvious to one of ordinary skill in the art at the time the invention was made to apply the teaching of Geva into the system of Miller because it would allow handling advanced loads in a cache system; thereby, increasing the performance and speed processing of the system.

7. In the Argument, the Appellant argued (7) that there is no suggestion to combine the teaching of Miller and Hale.

In response to Appellant's arguments (7) that there is no suggestion to combine the references, the examiner recognizes that obviousness can only be established by combining or modifying the teachings of the prior art to produce the claimed invention where there is some teaching, suggestion, or motivation to do so found either in the references themselves or in the knowledge generally available to one of ordinary skill in the art. See *In re Fine*, 837 F.2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988)and *In re Jones*, 958 F.2d 347, 21 USPQ2d 1941 (Fed. Cir. 1992). In this case, Miller does not

explicitly show said writing step is initiated by executing a specific machine specific instruction. Hale shows writing step initiated by executing a specific machine specific instruction (e.g., col. 9, lines 30-45). It would have been obvious to one of ordinary skill in the art at the time the invention was made to apply the teaching of Hale into the system of Miller because it would allow a secure boot process when performing initialization of a computer system upon power up or system reset.

8. In the arguments; the appellant argued (8) that there is no suggestion to one ordinary skill in the that Miller's method for handling invalid data in a memory is combinable with Hale's method for initializing a computer system.

The examiner disagreed with the appellant's argument (8) because both Miller and Hale teach data invalidate at initialization. In particular, Miller teaches data invalidate at initialization (e.g., col. 15, lines 35-60) and Hale teaches data invalidate at initialization (e.g., fig. 3, els. 310, 320col. 9, lines 30-45).

Also, Miller does not explicitly show said writing step is initiated by executing a specific machine specific instruction and Hale shows writing step initiated by executing a specific machine specific instruction (e.g., col. 9, lines 30-45). Therefore, Miller and Hale suggest the desirability of the combination. It would have been obvious to one of ordinary skill in the art at the time the invention was made to apply the teaching of Hale into the system of Miller because it would allow a secure boot process when performing initialization of a computer system upon power up or system reset.

(11) Related Proceeding(s) Appendix

No decision rendered by a court or the Board is identified by the examiner in the Related Appeals and Interferences section of this examiner's answer.

For the above reasons, it is believed that the rejections should be sustained.

Respectfully submitted,

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PPE 2185

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